

2-1	2-1
Class	Subclass

**ISSUE CLASSIFICATION**

PATENT NUMBER

## U.S. REISSUE PATENT APPLICATION

DB	O.I.P.E.	O.G. PUBLICATION DATE	REISSUE PATENT DATE
SCANNED <i>TRC</i>	O.A. <i>SAH</i>	5-5-51	

APPLICATION NO. 09/328910	CONT/PRIOR D F	CLASS 257	SUBCLASS	ART UNIT 2811	EXAMINER J. Lee R.
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LEADFRAME SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE USING THE SAME  
AND METHOD OF AND PROCESS FOR FABRICATING THE TWO

PTO-2040  
12/89

☐ SURRENDER OF ORIGINAL PATENT

**Exp. 100000**

**PREPARED AND APPROVED FOR ISSUE**

**ISSUING CLASSIFICATION**

[illegible]

<input checked="" type="checkbox"/> <b>TERMINAL DISCLAIMER</b>	<b>DRAWINGS</b>			<b>CLAIMS ALLOWED</b>	
	Sheets Drawn 21	Figs. Drawn 35	Print Figs. 24, 25	Total Claims 89	Print Claim for O.G. 1
<input checked="" type="checkbox"/> The term of this patent subsequently <u>                    </u> (date) has been disclaimed.	_____ (Assistant Examiner) (Date)			<b>NOTICE OF ALLOWANCE MAILED</b>	
<input checked="" type="checkbox"/> The term of this patent shall not extend beyond the expiration date of Pat. No. _____.	_____ (Assistant Examiner) (Date)			<b>ISSUE FEE</b>	
<input type="checkbox"/> The terminal _____ months this patent have been disclaimed.	JASMINE J B CLARE 3/7/02 _____ (Primary Examiner) (Date)			Amount Due	Date Paid
<b>FINAL SPRE REVIEW</b>	_____ (Legal Instruments Examiner) (Date)			<b>ISSUE BATCH NUMBER</b>	
_____ (INITIALS)	_____ (Date)			_____ (Date)	

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(LABEL AREA)

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